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(cont'd)

output. Then, the correction adder 83 adds the lower 2 bits of the correction address PC and the upper tenth bit and eleventh bit (PDL14, PDL15) of the 24-bit in-quadrant division unit address PDL, to thereby output one wavelength division unit address AD (AD0, AD1).--

IN THE CLAIMS

Please amend claims 1-5, 9-10, 12-14, and 16-17 by rewriting same to read as follows:

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--1. (Twice Amended) A position detection apparatus comprising:

a recording medium on which a periodic position signal is recorded;

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a detection section having a first detection head that moves relative to said recording medium along a recording direction of said position signal for detecting said position signal and a second detection head disposed apart from said first detection head by a predetermined distance along said recording direction of said position signal that moves relative to said recording medium and that operates with said first detection head for detecting said position signal;

a polar conversion section for converting said position signal detected by said first detection head and said second detection head into an angle signal that represents a relative position of said recording medium and said detection section as an angle;

a low pass filter for removing a high frequency component

in said angle signal output from said polar conversion section to output an angle signal having a frequency such that a phase error is zero; and

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an output section for outputting relative position information of said recording medium and said detection section based on said smoothed angle signal from which said high frequency component has been removed by said low pass filter.

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(contd)
--2. (Twice Amended) The position detection apparatus according to claim 1, wherein said low pass filter comprises:

a frequency control oscillator for outputting a periodic signal having a frequency controlled based on a frequency control signal;

a phase comparator for comparing a phase of said angle signal output from said polar conversion section and said periodic signal output from said frequency control oscillator to output said phase error;

first gain-controllable amplifier means for one of increasing and decreasing said phase error output from said phase comparator;

second gain-controllable amplifier means for one of increasing and decreasing said phase error output from said first amplifier means;

an integrator for integrating said phase error output from said second gain-controllable amplifier means to output a velocity error; and

an adder for adding said velocity error output from said integrator and said phase error output from said first gain-

controllable amplifier means to generate said frequency control signal,

wherein said frequency control oscillator controls said frequency of said periodic signal such that said phase error is zero based on said frequency control signal and outputs said periodic signal as said smoothed angle signal from which said high frequency component has been removed.

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--3. (Twice Amended) The position detection apparatus according to claim 2, wherein said integrator integrates said phase error increased or decreased by said second gain-controllable amplifier means; and

said adder adds said velocity error output from said integrator and said phase error output from said first gain-controllable amplifier means.

--4. (Twice Amended) The position detection apparatus according to claim 2, further comprising a prediction section having a prediction section adder that adds said velocity error output from said integrator in said low pass filter and said smoothed angle signal output from said frequency control oscillator,

wherein said output section outputs said relative position information of said recording medium and said detection section, based on a signal output from said prediction section.

--5. (Twice Amended) The position detection apparatus according to claim 4, wherein said prediction section has

third gain-controllable amplifier means for increasing or decreasing said velocity error output from said integrator in said low pass filter; and

said prediction section adder adds said smoothed angle signal output from said frequency control oscillator and a velocity error output from said third amplifier means.

--9. (Twice Amended) The position detection apparatus according to claim 8, wherein said gain control section controls said gain of said phase error output from said phase comparator depending on a size of said phase error and/or a frequency of said phase error.

--10. (Twice Amended) The position detection apparatus according to claim 8, said polar conversion section generating an amplitude signal together with said angle signal and comprising:

a noise detection section for detecting inside noise based on said amplitude signal and/or said phase error,

wherein said gain control section decreases said gain of said phase error output from said phase comparator when external noise occurs or said noise detection section detects noise.

--12. (Twice Amended) The position detection apparatus according to claim 8, wherein said gain control section decreases said gain of said phase error when an absolute value of said phase error output from said phase comparator exceeds a predetermined level.

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--13. (Twice Amended) The position detection apparatus according to claim 12, wherein said gain control section decreases said gain of said phase error when said condition that said absolute value of said phase error output from said phase comparator exceeds said predetermined level for a predetermined time.

--14. (Twice Amended) The position detection apparatus according to claim 1, wherein said polar conversion section designates said position signal detected by said first detection head and said second detection head as an address, and uses a table within which said angle signal corresponding to said address is stored to generate said angle signal representing said relative position of said recording medium and said detection section as said angle.

--16. (Twice Amended) An arithmetic processing unit comprising:

B9

a polar conversion section for converting a first periodic signal and a second periodic signal whose phase is different from that of said first periodic signal into an angle signal showing an angle of said first periodic signal and said second periodic signal;

a low pass filter for removing a high frequency component in said angle signal output from said polar conversion section to output an angle signal having a frequency such that a phase error is zero; and

an output section for outputting position information

shown by said first periodic signal and said second periodic signal, based on said angle signal from which said high frequency component has been removed by said low pass filter.

--17. (Twice Amended) The arithmetic processing unit according to claim 16, wherein said low pass filter comprises:

a frequency control oscillator for outputting a periodic signal having a frequency controlled based on a frequency control signal;

a phase comparator for comparing a phase of said angle signal output from said polar conversion section and said periodic signal output from said frequency control oscillator to output said phase error;

an integrator for integrating said phase error output from said phase comparator to output a velocity error; and

an adder for adding said velocity error output from said integrator and said phase error output from said phase comparator to generate said frequency control signal, wherein said frequency control oscillator controls said frequency of said periodic signal such that said phase error is zero based on said frequency control signal, and outputs said periodic signal as said angle signal from which said high frequency component has been removed.--

REMARKS

Claims 1-17 remain in the application, and claims 1-5, 9-10, 12-14, and 16-17 have been amended hereby.

The Claims have been carefully reviewed and amended with